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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,283	08/06/2003	Tyson R. McGuffin	200208596-1	1374

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,283	MCGUFFIN ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *13-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/635283 file on 08/06/03. The examiner acknowledges: the election of group I claims 1-12 without traverse. The withdraw of non-election claims 13-29.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 1 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The recited limitations "area data associated with transistor gate area of at least one unit of a circuit design" and "a power estimation engine that determines a relative estimation of power for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area" are just abstract ideas. The claim limitations do not specifically disclose what is area data associated with transistor gate area of at least one unit of a circuit design and how to use power estimation engine that determines a relative estimation of power for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area. Thus the claim invention has no concrete result.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Khouja et al. (US Patent 6075932).

3. As to claim 1, Khouja et al. teach a power estimation system, comprising: area data associated with transistor gate area of at least one unit of a circuit design (see fig 2B col 4 lines 51 to col 6 lines 64); and a power estimation (see col 10 lines 15-19) engine that determines a relative estimation of power (see col 4 lines 51 to col 6 lines 63) for the at least one unit of the circuit design based on a predetermined correlation that characterizes device power as a function of transistor gate area (see fig 2 col 10 lines 15 to col 11 lines 35 and col 4 lines 51 to col 6 lines 63 and col 23 lines 4 to col 25 line 38 and col 37 line 56 to col 39 lines 58).

4. As to claim 2, Khouja et al. teach the power estimation engine determines the relative estimation of power by employing at least one coefficient that characterizes device power as a function of transistor gate area (see fig 2B col 4 lines 51 to col 6 lines 64 and col 23 lines 4 to col 25 line 38 and col 37 line 56 to col 39 lines 58).

5. As to claim 3, Khouja et al. teach the at least one coefficient defining a substantially linear relationship between device power and transistor gate area, such that the at least one coefficient includes a multiplier coefficient and an offset coefficient (see fig 2B col 4 lines 51 to col 6 lines 64 and col 23 lines 4 to col 25 line 38 and col 37 line 56 to col 39 lines 58).

6. As to claim 4, Khouja et al. teach the relative estimation of power is based on a determination of static power and dynamic power (see col 2 lines 65 to col 5 lines 64).

7. As to claim 5, Khouja et al. teach the relative estimation of power is based on a determination of gate leakage power (col 10 lines 20-34).

8. As to claim 6, Khouja et al. teach the area data comprising high voltage threshold (HVT) transistor gate area data and low voltage threshold (LVT) transistor gate area data (see col 4 lines 50 to col 5 lines 63).

9. As to claim 7, Khouja et al. teach the power estimation engine employs a first predetermined correlation of power based on HVT transistor gate area data that characterizes HVT device power as a function of HVT transistor gate area and a second predetermined correlation of power based on LVT transistor gate area that characterizes LVT device power ms a function of LVT transistor gate area (see col 4 lines 50 to col 5 lines 63).

10. As to claim 8, Khouja et al. teach the first predetermined correlation being a first set of at least one coefficient that characterizes HVT device power as a function of HVT transistor gate area and the second predetermined correlation being a second set of at least one coefficient that characterizes LVT device power as a function of LVT transistor gate area, the relative estimation of power for the at least one unit of the circuit design is computed by adding the power determined for the HVT devices and the power determined for the LVT devices (see col 4 lines 50 to col 5 lines 63).

11. As to claim 9, Khouja et al. teach the estimation of power for the at least one unit of the circuit design being further computed by adding a gate leakage power estimation based on both the HVT transistor gate area and the LVT transistor gate area and a third set of at least one coefficient based on a predetermined correlation that characterizes gate leakage power as a function of HVT transistor gate area and LVT transistor gate area (see col 4 lines 50 to col 5 lines 63).

12. As to claim 10, Khouja et al. teach further comprising an area calculator that generates the area data by analyzing a netlist provided by an optimization tool (col 11 lines 36-63).

13. As to claim 11, Khouja et al. teach the area calculator and the power estimation engine cooperate with the optimization tool to generate a plurality of relative power estimates based on a plurality of circuit sizing instances of the at least one unit of the circuit design, the plurality of relative power estimates having a relative relationship to one another based on the predetermined correlation (see fig 3-5 col 10 line 31 to col 11 lines 35).

14. As to claim 12, Khouja et al. teach, the correlation of power with respect to transistor gate area is determined by analyzing power data and associated transistor gate area data based on a plurality of instances of at least one circuit design type (see col 4 lines 50 to col 5 lines 63 and background).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BINH TAT

SEPTEMBER 2, 2006

Thuando
THUAN DO
Primary examiner
09/05/06